						REV	DATE		REVIS	
INPUT						-	03-03-14	Initial Rel	lease	
Frequency										
10 MHz GPS	S, sine									
Input Level										
+7 dBm ±5 c	IB into 50 c	hms								
OUTPUT						Spurio	ous			
Frequency/Out	put Level					≤-8	0 dBc, exc	luding p	bower s	
10 MHz GPS	6 (return), +	POWER REQUIREMENTS								
20 MHz; +13	$dBm \pm 2 d$		Supply Voltage							
40 MHZ; +13	aBm ±2 a	+18 VDC ±5%								
80 MHZ; +13	(Regulated to +15 VDC on p									
100 MHZ, +1	Warm-Up Power									
520 MHZ, +1	< 35 Watts for 10 minutes at									
1200 MU	Total Power									
1280 MHz; +13 dBm ±2 dB into 50 ohms 2560 MHz; +13 dBm ±2 dB into 50 ohms						< 29 Watts at +25°C				
5120 MH ₇ · 1	13 dRm ±2	dB into 50	ohme			ADJUSTMENT				
10240 MH7	+13 dRm +	-2 dB into 50) ohme			Loop BW (Locking to external				
STABILITY			5 Onnio			Target Bandwidth: ≤ 10 Hz				
Aging (free-rur	Type 2 Loop									
1×10^{-6} first										
-7	year aller .	so days ope	rating, typ	ical						
5 x 10 _ seco	ond year, ty	/pical								
3 x 10 ⁻⁷ per	vear therea	after, typical				MECH				
Phase Noise L	(f). dBc/Hz	. free-runni	na			Раска	ge moduloo c		llotorm	
	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	RF	modules a	ina oscii Im plata	nator m	
20 MH 7	-110	-140	-160	-165	-165	Dimon	an alumin sions	in plate	1	
	-104	-134	-150	-165	-165	12"	v 18" v 3"	may (A	octual e	
	100	120	159	172	17/	Conne		, шах (л	ictual 3	
	-100	-130	-150	-175	-174	RF	Input/Outr	outs: SM	1A(f) Io	
160 MHZ	-92	-122	-150	-165	-100		Power: Te	erminal h	olock	
320 MHz	-86	-116	-144	-159	-160	Mount	ina		51001	
640 MHz	-80	-110	-138	-153	-154	Thr	u holes on	plate. 0).166" c	
1280 MHz	-73	-103	-131	-146	-147	OTHE	R	p, .		
2560 MHz	-67	-97	-125	-140	-141	Test D	ata			
5120 MHz	-61	-91	-119	-133	-134	Out	put Levels	, Phase	Noise	
10240 MHz	-54	-84	-112	-127	-128	Har	monics, S	ubs, Pro	oducts,	
Temperature S	tability							Nonz	ما ۸د	
±5 x 10 ⁻⁷ , 0	to +50°C (F	Ref. +25°C),	free-runni	ng						
Harmonics						Title:	10 00 11	so 220	640 4	
≤ -25 dBc						20	, 40, 80, 10	50, 320, F	040, 1/	
Sub-Harmonic	S					₽/N·		Rev [.]	Date:	
≤ -60 dBc						50	1-26733	-	03-	
PLL Divider Pr	oducts						. 20100			
≤ -60 dBc						Tolerance (except as	s: noted)	0.XX Dec:	2 0 "	
						Dimension	s are in inches			

REV	DATE		REVISION RECOR	D	DWN	AUTH							
-	03-03-14	Initial Rele	ease		PAC								
					1								
purio	us												
≤ -80	≤ -80 dBc, excluding power supply line related spurs												
OWE	OWER REQUIREMENTS												
upply	Voltage												
+18	VDC ±5%)											
(Reg	(Regulated to +15 VDC on plate)												
arm-	arm-Up Power												
< 35	< 35 Watts for 10 minutes at +25°C												
otal P	otal Power												
< 29	Watts at	+25°C											
DJUS	DJUSTMENT												
оор В	oop BW (Locking to external 10 MHz reference)												
Targ	Target Bandwidth: ≤ 10 Hz												
Туре	Туре 2 Loop												
RYST	AL												
ype													
80 N	80 MHz SC-Cut												
ECH/	ANICAL												
ackag	je												
RF r	modules a	nd oscill	ator mounted										
on a	n aluminu	m plate											
imens	sions		–										
12" :	12" x 18" x 3", max (Actual size TBD)												
onne	ctors		A (6)										
RFI	RF Input/Outputs: SMA(f), located on first/last module in string												
DC	DC Power: Terminal block												
ounti	ounting												
Thru	I holes on	plate, 0	.166" diam., 14	places									
THER	(
est Da	ata		Nutria										
Output Levels, Phase Noise													
Harr	monics, Su	ibs, Pro	aucts, Spuriou	S									
		N/ -		4.a									
Wenzel Associates, Inc. Austin, Texas													
20, 40, 80, 160, 320, 640, 1280, 2560, 5120 and 10240 MHz PL Plate Assembly													
?/N:		Rev:	Date:	Drawn:	Ref:								

03-03-14

0.XXX Dec:

±0.010"

FSCM:

62821

Ref: 23914b

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