

REV	DATE	REVISION RECORD	DWN	AUTH
-	02-07-11	Draft	VG	JR
A	02-15-11	Revised phase noise spec	VG	RTK

**INPUT**

**Frequency**

10 MHz,  $\pm 2 \times 10^{-6}$

**Level**

+7 dBm  $\pm 5$  dB into 50 ohms

**OUTPUT**

**Frequency**

100 MHz

**Level**

+13 dBm  $\pm 2$  dB into 50 ohms

**STABILITY**

**Output Phase Noise L(f)**

**(Free-Running)**

- 100 Hz -128 dBc/Hz
- 1 kHz -155 dBc/Hz
- 10 kHz -170 dBc/Hz
- 100 kHz -171 dBc/Hz

**Aging**

$\pm 1 \times 10^{-6}$  per year after 30 days operating, typical

**Temperature Stability**

$\pm 5 \times 10^{-7}$  free-running from 0 to +50°C, (Ref. +25°C)

**Phase Lock Alarm**

TTL  
 Locked: +3.5 VDC to +5.2 VDC (Hi)  
 Out-of-Lock: +0.8 VDC max (Lo)

**Phase Lock Voltage Monitor**

Voltage monitor pin supplied

**SPECTRAL PURITY**

**Harmonics**

$\leq -30$  dBc

**Sub-Harmonics**

$\leq -50$  dBc

**PLL Divider Products**

$\leq -60$  dBc

**Spurious**

$\leq -70$  dBc

**MECHANICAL**

**Dimensions**

2.5 x 3.5 x 0.8"

**Connectors**

SMA's and solder pins on side  
 Feed-thru terminals for lock alarm, supply and phase lock voltage monitor

**Packaging**

Nickel-plated machined aluminum housing

**Mounting**

Tapped holes on sides, 16 places  
 Through holes, 4 places  
 Threaded inserts on base, 4 places

**POWER REQUIREMENTS**

**Supply Voltage**

+15 VDC  $\pm 5\%$

**Warm-Up Power**

$\leq 8$  Watts at start-up for 5 minutes at +25°C

**Total Power**

$\leq 5$  Watts at steady state +25°C

**ADJUSTMENT**

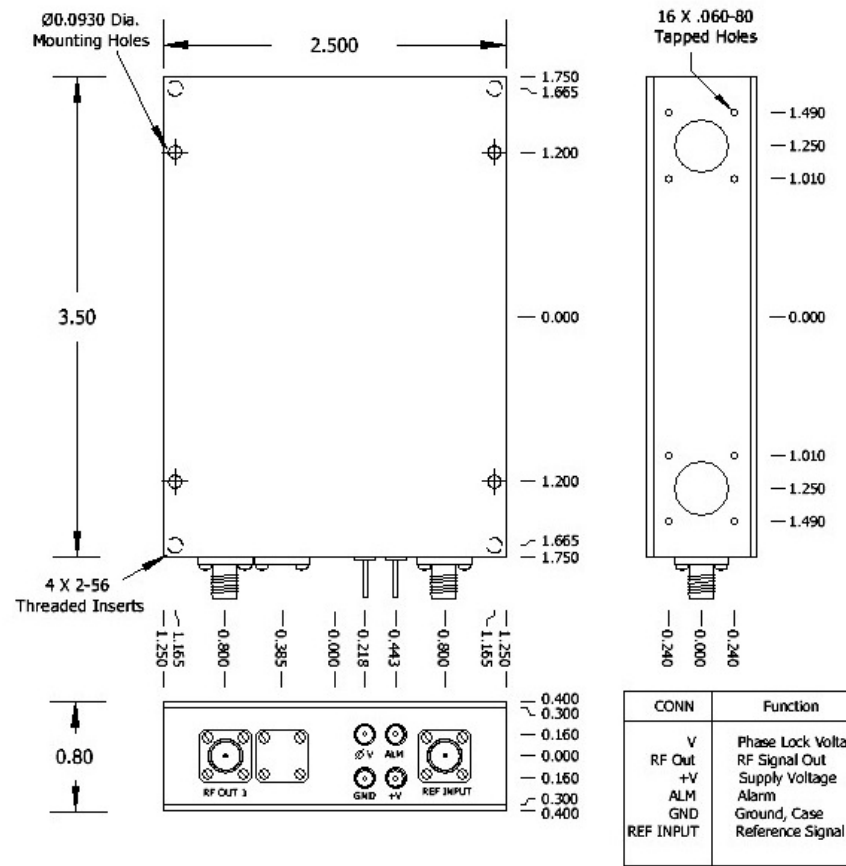
**Loop BW**

Target Bandwidth: 60 Hz  
 Type 2 Loop

**CRYSTAL**

**Type**

SC-cut



**Wenzel Associates, Inc.**

Austin, Texas

Title: **Standard 100 MHz-SC Phase Lock Crystal Oscillator**

P/N: <b>501-23588</b>	Rev: <b>A</b>	Date: <b>02-15-11</b>	Drawn:	Ref: SPR
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Tolerances: (except as noted) Dimensions are in inches	0.XX Dec: <b><math>\pm 0.030</math>"</b>	0.XXX Dec: <b><math>\pm 0.010</math>"</b>	FSCM: <b>62821</b>	Page 1 of 1
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