

Bootstrapping a Phase Locked Loop for Better Performance

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Introduction

This paper describes a bootstrapping technique for phase locked loops to improve the oscillators' performance¹. The compensation scheme may be useful for correcting aging, warm-up characteristics, temperature stability, short-term stability, and vibration induced phase noise. Unlike other multi-crystal or multi-oscillator schemes, this approach does not require unusual mechanical configurations or special sensors and the oscillators are phase locked eliminating low frequency spurious "beat notes".

General Concept

Fig. 1 depicts an ordinary PLL and a possible bootstrapped PLL implementation. A PLL's correction voltage is proportional to the frequency difference that would be present if the oscillators were unlocked (assuming linear tuning). If the frequency difference is a linear and repeatable externally induced effect or a linear time related effect then this correction voltage may be used to generate a compensating signal. The properly scaled compensation is applied with the same polarity to the electrical tuning of both oscillators bootstrapping their frequencies by the same amount. By bootstrapping both oscillators, the phase locked loop remains unaffected and the linear perturbation is removed. Non-linear frequency perturbations may also be compensated but the compensating signal will require non-linear processing instead of simple scaling. The technique requires that the two oscillators have significantly different sensitivities to the external influence but in practice, it is usually easier to find crystals with different aging rates, acceleration sensitivities, or frequency hops than to find matched crystals.

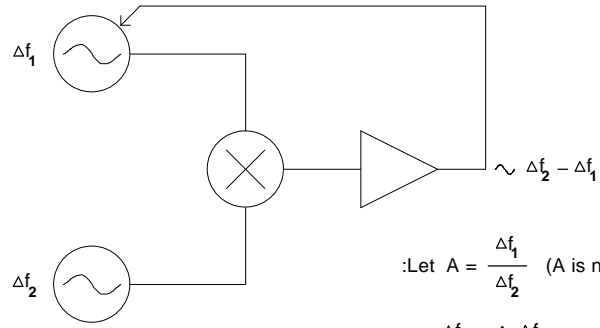
Aging Correction

A simple aging correction system serves as an example of the technique. Assume that the two phase locked oscillators have predictable aging rates of +2 PPM and +5 PPM per year and assume that the tuning sensitivity of their electrical tuning is 1 PPM per volt. When the two oscillators are phase locked, the tuning voltage will vary at a rate of 3 volts per year (3 PPM difference per year). If the 2 PPM oscillator is the master in the PLL then scaling the tuning voltage by $-2/3$ will give the correction voltage needed to remove the aging from the reference ($3 \times 2/3 = 2$ volts per year). If the other oscillator is the reference then the scale factor would be selected to be $-5/3$. The negative polarity is accomplished by the summing amplifiers in fig. 1. Applying the scaled voltage to both oscillators will eliminate the aging of both without disturbing the PLL. After a year of operation, the voltage on the tuning of the 2 PPM oscillator will have dropped by 2 volts and the voltage on the 5 PPM oscillator will have dropped by $3 + 2 = 5$ volts. Obviously, this technique requires predictable and stable aging rates and would therefore have limited usefulness in this application.

Vibration Compensation

A more appropriate application is the correction of vibration induced phase noise. Quartz crystals exhibit a direction-dependent sensitivity to acceleration resulting in induced phase noise in the presence of vibration. Earlier compensation schemes attempted to model the sensitivity, direction and

¹ Although this material is believed to be original, the originality of the concepts presented here is unknown and existing patents may cover some portion of the presented material.



:Let $A = \frac{\Delta f_1}{\Delta f_2}$ (A is not near 1.)

$\Delta f_1 = A \Delta f_2$

$\Delta f_2 - \Delta f_1 = (1-A) \Delta f_2$

$\frac{\Delta f_2 - \Delta f_1}{-(1-A)} = -\Delta f_2$ (This is the necessary correction signal.)

↗
scale factor
(note that A must not equal 1)

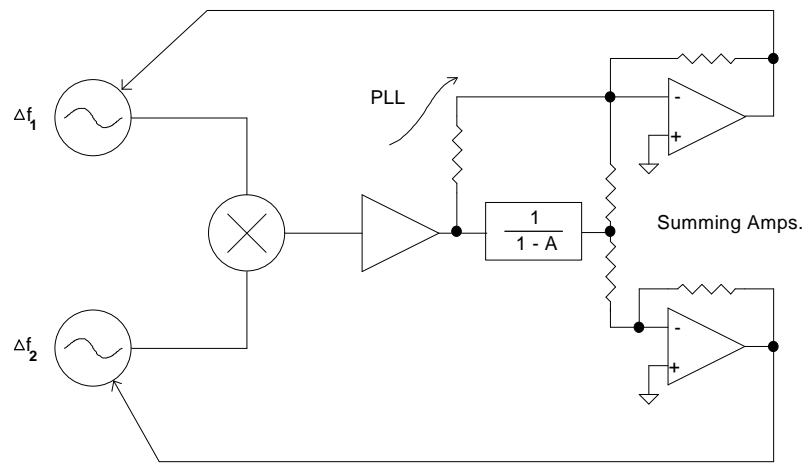


Figure 1: Bootstrapped PLL reduces oscillator instabilities.

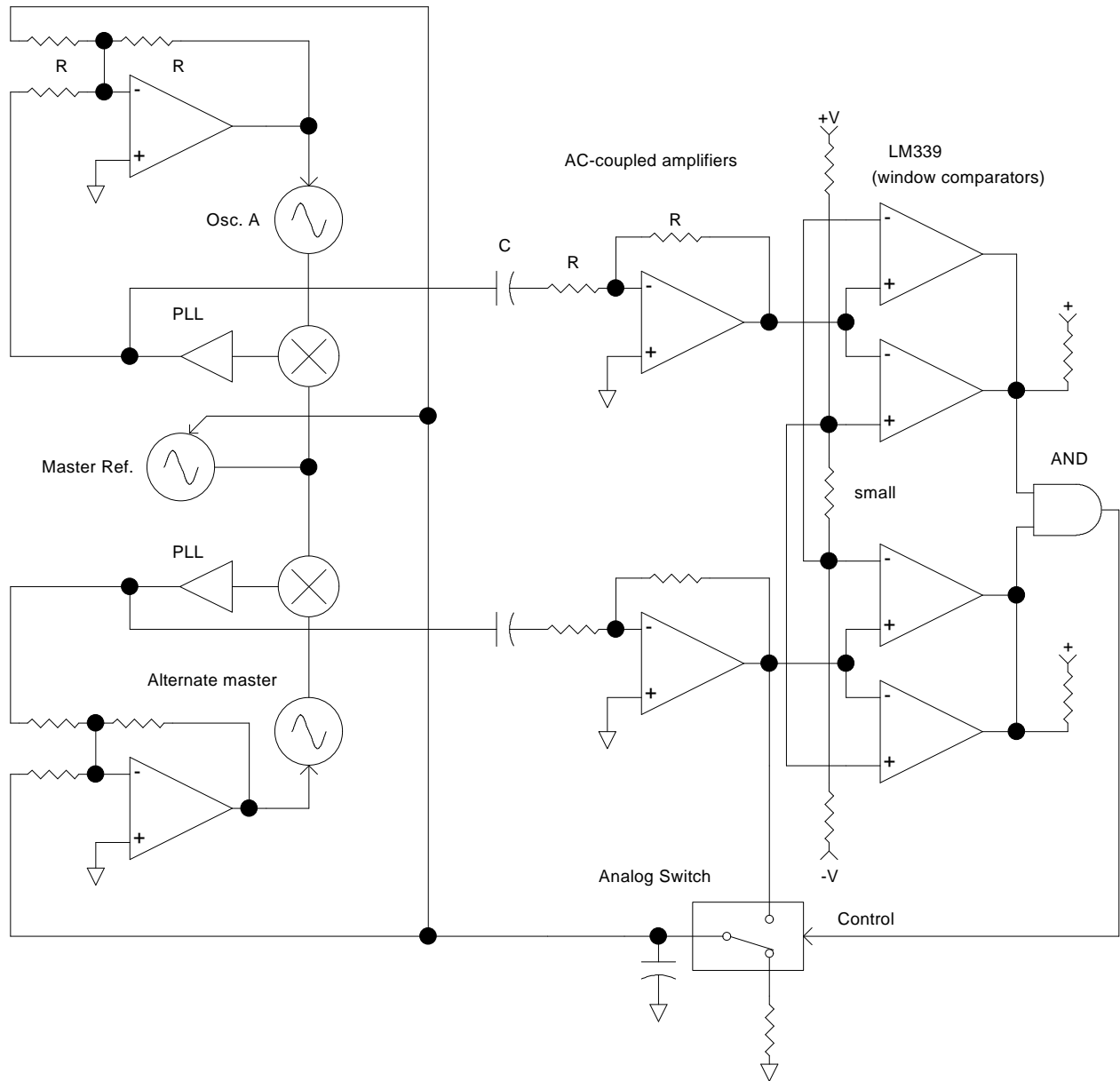


Figure 2: Bootstrapped reference oscillator moves slowly to a new frequency instead of jumping.

resonances of the crystal's acceleration sensitivity vector with accelerometers but these systems can be quite involved. Another technique mounts crystals exhibiting similar sensitivities with the acceleration vectors pointing in the opposite direction. In a special oscillator circuit, the sensitivity to vibration is significantly reduced but the crystal mounting and matching are both difficult. The bootstrapping technique shown in fig. 1 requires crystals with *different* acceleration sensitivities, an easily met requirement. Also, the crystals are simply mounted side-by-side with the acceleration vectors pointing in the same direction. If the sensitivities are different, a fast PLL's tuning voltage will vary in proportion to this difference and the vibration level. By scaling this voltage and applying it to both oscillators the vibration sensitivity is reduced.

Frequency Hops

Another application for the bootstrapped PLL is the combining of three oscillators to slow the occasional frequency steps exhibited by many precision crystals. Sudden steps of a few parts per billion can destabilize certain timing receivers. Previous schemes have combined three free-running oscillators with frequency discriminators in a voting arrangement to determine which oscillators are in closest agreement. The oscillator exhibiting the most frequency deviation is ignored and one of the other two oscillators is used for the output. In the proposed bootstrapped PLL scheme, the three oscillators are phase locked and the tuning voltages are monitored to determine which oscillator has taken a frequency step (fig. 2). One oscillator is arbitrarily chosen as the master and another is chosen as the alternate master. In operation, the master controls the output frequency via the two PLLs. If the master takes a frequency step then both of the PLLs will exhibit a voltage step triggering the comparators and gate. The gate output toggles the analog switch connecting the output of alternate master's PLL to the bootstrap inputs canceling the step induced by the master. The tuning voltage is AC coupled into the comparators so that the system only responds to sudden steps and reverts back to the nominal state after a period of time. Since the bootstrapping voltage is applied to both oscillators, the PLLs are not disturbed. If either of the other two oscillators takes a frequency step, the AND gate does not toggle and the master remains in control. The net result is to smooth the master oscillator's frequency steps, converting them to a frequency drift slow enough to be tolerated by timing receivers.

Conclusion

Phase locked loops may be shifted in frequency without disturbing the loop if both oscillators are tuned by the same amount. The presented technique extracts information about undesirable oscillator behavior from a PLL's tuning voltage and bootstraps both oscillators to reduce the behavior. The bootstrapping technique may find other applications including loop-independent FM modulation and rapid tuning of slow loops and multiple-loop systems.

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